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10/759,297	01/20/2004	Shunpei Yamazaki	0756-7251	7182

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,297	SHUNPEI YAMAZAKI	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2 and 7-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sarma et al (U.S. 5,258,323) in view of M. Bruel (Article "Silicon on insulator material technology" IEE 1995).

As to claim 1, Sarma et al discloses in figures 4a-4g a semiconductor device and a corresponding method of manufacturing a semiconductor device, the method comprising the steps of: forming a silicon island (34) by patterning the single crystal silicon film ("single crystal silicon device layer") (col. 3, lines 64-65); and thermally oxidizing the silicon island in order to eliminate trap levels and defects from the silicon island (col. 4, lines 1-10).

Sarma et al does not disclose a semiconductor device and a corresponding method of manufacturing a semiconductor device, comprising a smart-cut process for forming a silicon island (a smart-cut process comprising the steps of: forming a hydrogen added layer by adding hydrogen to a first single crystal silicon substrate from a major surface side thereof, said first single crystal substrate having a silicon oxide film on the major surface; bonding the first single crystal silicon substrate to a second substrate through the silicon oxide film with a bonded interface therebetween, said second substrate being as a support; separating the first single crystal silicon substrate by a first heat treatment; carrying out a second heat treatment to a single

crystal silicon film which remains on the second substrate in the separating step so that the bonded interface becomes stable; flattening a major surface of the single crystal silicon film).

Bruel (IEE 1995) discloses in figure 1 the method of using a principle of smart-cut process for forming a silicon island, the method comprising the steps of: forming a hydrogen added layer by adding hydrogen to a first single crystal silicon substrate from a major surface side thereof, the first single crystal substrate having a silicon oxide film on the major surface (see Fig.1, "step 1"); bonding the first single crystal silicon substrate to a second substrate through the silicon oxide film with a bonded interface therebetween, said second substrate being as a support (see Fig.1, "step 2"); separating the first single crystal silicon substrate by a first heat treatment ["first phase" (400-600 °C)] (see page 1201); carrying out a second heat treatment ["second phase" (>1000°C)] (see page 1201) to a single crystal silicon film which remains on the second substrate in the separating step so that the bonded interface capable of becoming stable (see Fig.1, "step 3"); flattening a major surface of the single crystal silicon film (see Fig.1, "step 4"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of manufacturing a semiconductor device of Sarma et al by using a principle of smart-cut process for forming a silicon island as taught by Bruel (IEE 1995) for achieving thin uniform SOI layers or providing major specific advantages (see pages 1201 and 1202 in Bruel).

As to claim 2, Sarma et al discloses in figures 4a-4g a semiconductor device and a corresponding method of manufacturing a semiconductor device, the method comprising the steps of: forming a silicon island (34) by patterning the single crystal silicon film ("single crystal silicon device layer") (col. 3, lines 64-65); and thermally oxidizing the silicon island so that the

bonded interface capable of becoming stable and trap levels and defects of the silicon island be eliminated (col. 4, lines 1-10).

Sarma et al does not disclose a semiconductor device and a corresponding method of manufacturing a semiconductor device, comprising a smart-cut process for forming a silicon island (a smart-cut process comprising the steps of: forming a hydrogen added layer by adding hydrogen to a first single crystal silicon substrate from a major surface side thereof, said first single crystal silicon substrate having a silicon oxide film on a major surface; bonding the first single crystal silicon substrate to a second substrate through the silicon oxide film, said second substrate being as a support; separating the first single crystal silicon substrate by a first heat treatment; flattening a major surface of a single crystal silicon film which remains on the second substrate in the separating step).

Bruel (IEE 1995) discloses in figure 1 the method of using a principle of smart-cut process for forming a silicon island, the method comprising the steps of: forming a hydrogen added layer by adding hydrogen to a first single crystal silicon substrate from a major surface side thereof, the first single crystal substrate having a silicon oxide film on the major surface (see Fig.1, "step 1"); bonding the first single crystal silicon substrate to a second substrate through the silicon oxide film, said second substrate being as a support (see Fig.1, "step 2"); separating the first single crystal silicon substrate by a first heat treatment ["first phase" (400-600 °C)] (see Fig. 1, "step 3", page 1201); flattening a major surface of the single crystal silicon film which remains on the second substrate in the separating step (see Fig.1, "step 4"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of manufacturing a

semiconductor device of Sarma et al by using a principle of smart-cut process for forming a silicon island as taught by Bruel (IEE 1995) for achieving thin uniform SOI layers or providing major specific advantages (see pages 1201 and 1202 in Bruel).

As to claims 7-16, Sarma et al in view of Bruel (IEE 1995) does not disclose a semiconductor device and a corresponding method of manufacturing a semiconductor device, wherein the semiconductor device is one selected from the group consisting of: a D/A converter, a Y correction circuit, and a signal dividing circuit; or one selected from the group consisting of a liquid crystal display device, an EL (electroluminescence) display device and an EC (electrochromic) display device; or a microprocessor; a computer for controlling a vehicle such as car or an electric train; or one selected from the group consisting of a video camera, a digital camera, a projector (rear type or front type), a head mount display (a goggle type display), a car navigation system, a personal computer, a portable information terminal such as a mobile computer, a portable telephone, or an electric book. However, the recited limitations above are intended use languages and they have been not given patentable weight, since it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ 2d 1647 (1987).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sarma et al in view of Bruel (IEE 1995) as applied to claims 1 and 2 above, and further in view of Linn et al (U.S. 5,387,555).

As to claims 3 and 5, Sarma et al in view of Bruel (IEE 1995) does not disclose a semiconductor device and a corresponding method of manufacturing a semiconductor device, wherein the thermally oxidizing step is carried out at a temperature in a range of from 1050 to 1150 degree C.

Linn et al (U.S. 5,387,555) discloses in figures 2C-6 a semiconductor device and a corresponding method of manufacturing a semiconductor device wherein the thermally oxidizing step is carried out at a temperature in a range of from 1050 to 1150 degree C ("1100 degree C" which is in the range of 1050 to 1150 degree C) (see col. 1, line 68 – col. 2, line 14). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of manufacturing a semiconductor device of Sarma et al in view of Bruel (IEE 1995) by applying a temperature in a range of from 1050 to 1150 degree C for thermally oxidizing step as taught by Linn et al for providing high quality thin silicon layers (see col. 1, line 68 – col. 2, line 14 in Linn et al).

5. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sarma et al in view of Bruel (IEE 1995) as applied to claims 1 and 2 above, and further in view of Zhang et al (U.S. 6,455,401).

As to claims 4 and 6, Sarma et al in view of Bruel (IEE 1995) does not disclose a semiconductor device and a corresponding method of manufacturing a semiconductor device, wherein the thermally oxidizing step is carried out in an oxidizing atmosphere comprising a halogen element.

Zhang et al (U.S. 6,455,401) discloses in figures 1A-3E a semiconductor device and a corresponding method of manufacturing a semiconductor device, wherein the thermally oxidizing step is carried out in an oxidizing atmosphere comprising a halogen element (see col. 23, lines 4-8). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of manufacturing a semiconductor device of Sarma et al in view of Bruel (IEE 1995) by having a thermally oxidizing step is carried out in an oxidizing atmosphere comprising a halogen element as taught by Zhang et al for increasing crystallinity of the at least one semiconductor island (see col. 23, lines 4-8).

Response to Arguments

6. Applicant's arguments filed 10/31/05 have been fully considered but they are not persuasive.

Applicant argued that the prior art does not teach or suggest "bonding the first single crystal silicon substrate to a second substrate through the silicon oxide film with a bonded interface therebetween, ... carrying out a second heat treatment to a single crystal silicon film which remains on the second substrate in the separating step so that the bonded interface becomes stable; ... thermally oxidizing the silicon island in order to eliminate trap levels and defects from the silicon island".

In response, the examiner disagrees with applicant's argument because Sarma et al clearly discloses in figures 4a-4g a semiconductor device and a corresponding method of manufacturing a semiconductor device, the method comprising the steps of: thermally oxidizing the silicon island in order to eliminate trap levels and defects from the silicon island (col. 4, lines 1-10). The above language of "in order to eliminate trap levels and defects from the silicon island" is the intended use language, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. Even though Sarma et al does not disclose the steps of: "bonding the first single crystal silicon substrate to a second substrate through the silicon oxide film with a bonded interface therebetween, ... carrying out a second heat treatment to a single crystal silicon film which remains on the second substrate in the separating step so that the bonded interface becomes stable". However, Bruel (IEE 1995) discloses in figure 1 the method of using a principle of smart-cut process having the steps of: bonding the first single crystal silicon substrate to a second substrate through the silicon oxide film with a bonded interface therebetween (it should be noted that: since first substrate is bonded to second substrate through the silicon oxide film, there is a bonded interface between them); carrying out a second heat treatment ["second phase" (>1000°C)] (see page 1201) to a single crystal silicon film which remains on the second substrate in the separating step *so that the bonded interface capable of becoming stable* (see Fig.1, "step 3"). The above language of "so that the bonded interface becomes stable" is the intended use language, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed

invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

ZANDRA V. SMITH
SUPERVISORY PATENT EXAMINER
01/01/2006